This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Previously Presented) An integrated circuit test apparatus, comprising;

at least one electrically conductive probe needle;

an optical scan mechanism arranged above the probe needle;

a holder adapted to receive a wafer while presenting a backside surface of the wafer upward to the optical scan mechanism and an opposing, frontside surface of the wafer downward to the probe needle; and

a mechanism coupled to the holder for moving the wafer relative to the probe needle.

2. (Original) The integrated circuit test apparatus of claim 1, further comprising a positioning camera arranged below the probe needle.

3. (Original) The integrated circuit test apparatus of claim 1, further comprising a probe card having trace conductors extending between the test device and the probe needle.

4. (Original) The integrated circuit test apparatus of claim 1, wherein the mechanism is adapted for movement in three dimensions relative to the probe needle, to enable the probe needle to contact a bonding pad upon an integrated circuit.

5. (Original) The integrated circuit test apparatus of claim 1, wherein the holder is adapted to receive an outer perimeter of the wafer frontside surface by applying vacuum pressure thereto.

6. (Original) The integrated circuit test apparatus of claim 1, wherein the holder is adapted to receive an outer perimeter of the wafer frontside surface by tabs arranged intermittently around the outer perimeter.

7. (Previously Presented) The integrated circuit test apparatus of claim 1, wherein the mechanism moves precisely the width of a die configured on the wafer from the die to each of all neighboring die across the entire wafer in a step-and-repeat fashion only during the interim between when the frontside and backside surfaces are presented to the probe needle and optical scan mechanism, respectively.

8. (Original) The integrated circuit test apparatus of claim 1, wherein the optical scan mechanism is adapted to emit radiation upon the backside surface and detect photoemission from the backside surface.

9. (Original) The integrated circuit test apparatus of claim 8, wherein the photoemission from the backside surface indicates the amount and/or location of defects on or near the frontside surface.

10. (Previously Presented) A method for testing an integrated circuit, comprising:

contacting a frontside surface of the wafer by a probe needle residing beneath the wafer;

exposing a backside surface of the wafer to an optical scan mechanism residing above the wafer; and

moving the wafer relative to the probe needle and scan mechanism precisely the width of a die configured on the wafer from the die to each of all neighboring die across the entire wafer in a step-and-repeat fashion during an interim between said contacting and said exposing.

11. (Original) The method of claim 10, wherein said contacting and said exposing occur concurrent with one another.

12. (Original) The method of claim 10, wherein said moving occurs via a machine.

13. (Original) The method of claim 10, wherein said contacting comprises:

connecting a test device to a bonding pad upon the frontside surface; and

activating the test device to apply or receive electrical energy to or from the bonding pad.

14. (Original) The method of claim 10, wherein said moving comprises retaining an outer perimeter of the wafer to a moveable holder that moves relative the probe needle and the scan mechanism.

15. (Original) The method of claim 10, further comprising measuring radiation emanating from the frontside surface, through the backside surface, and upon the scan mechanism.

16. (Original) The method of claim 15, wherein said contacting comprises forwarding electrical stimuli into the probe needle.

17. (Original) The method of claim 16, wherein said measuring occurs concurrent with said forwarding of electrical stimuli.

18. - 20. (Canceled)